HCAL Front End Electronics

Theresa Shaw

CMS HCAL Electronics Project Engineer

DOE/NSF Review

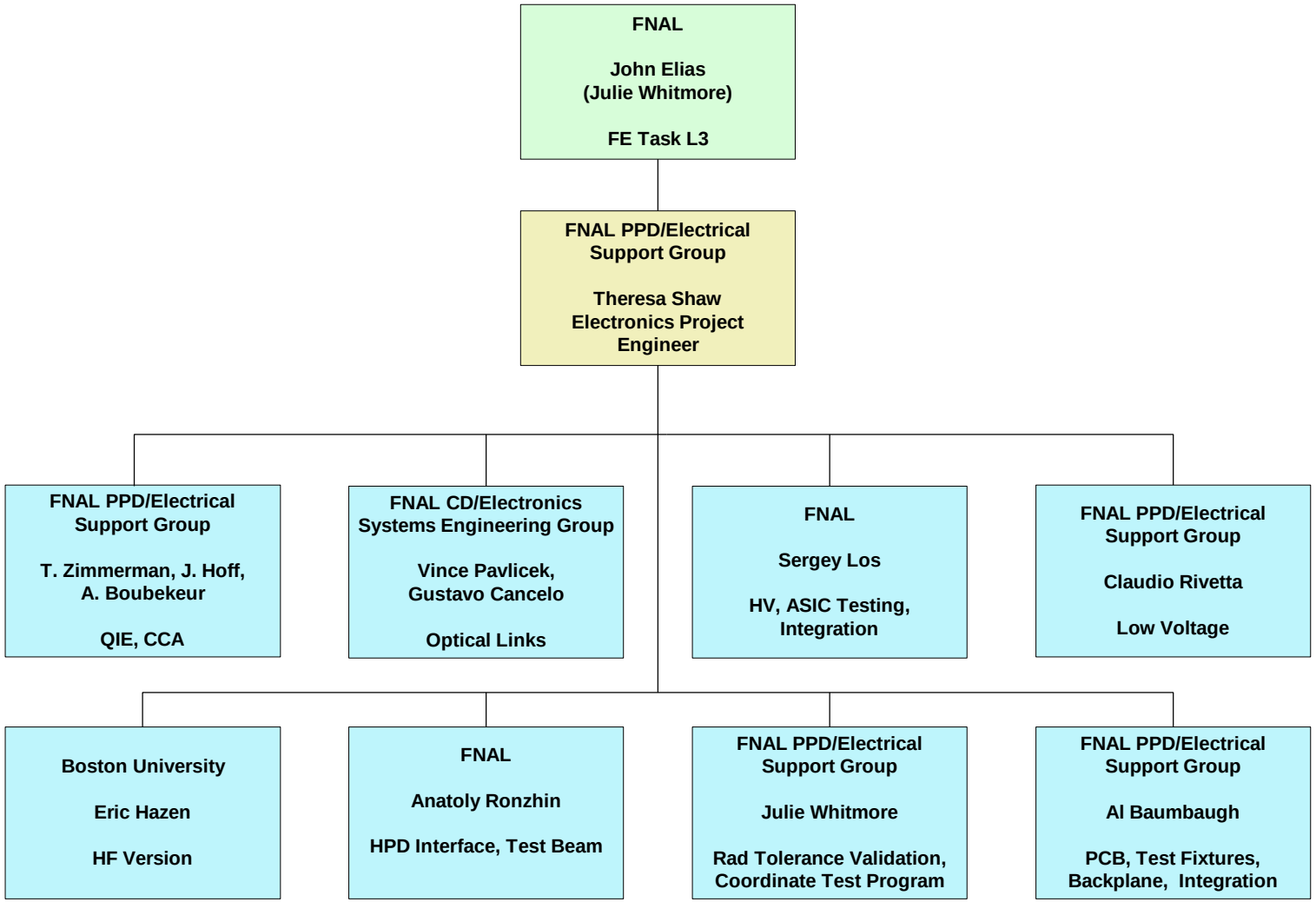
April 12, 2000

HCAL Electronics Topics

WBS 2.x.5 Front End Electronics

- QIE ASIC
- Channel Control ASIC
- Optical Transmitter
- Voltage Regulator
- 6 Channel Readout Module
- Readout Box Backplane
- Fiber Optic Cable
- Test Stands
- RAD Tolerance Validation

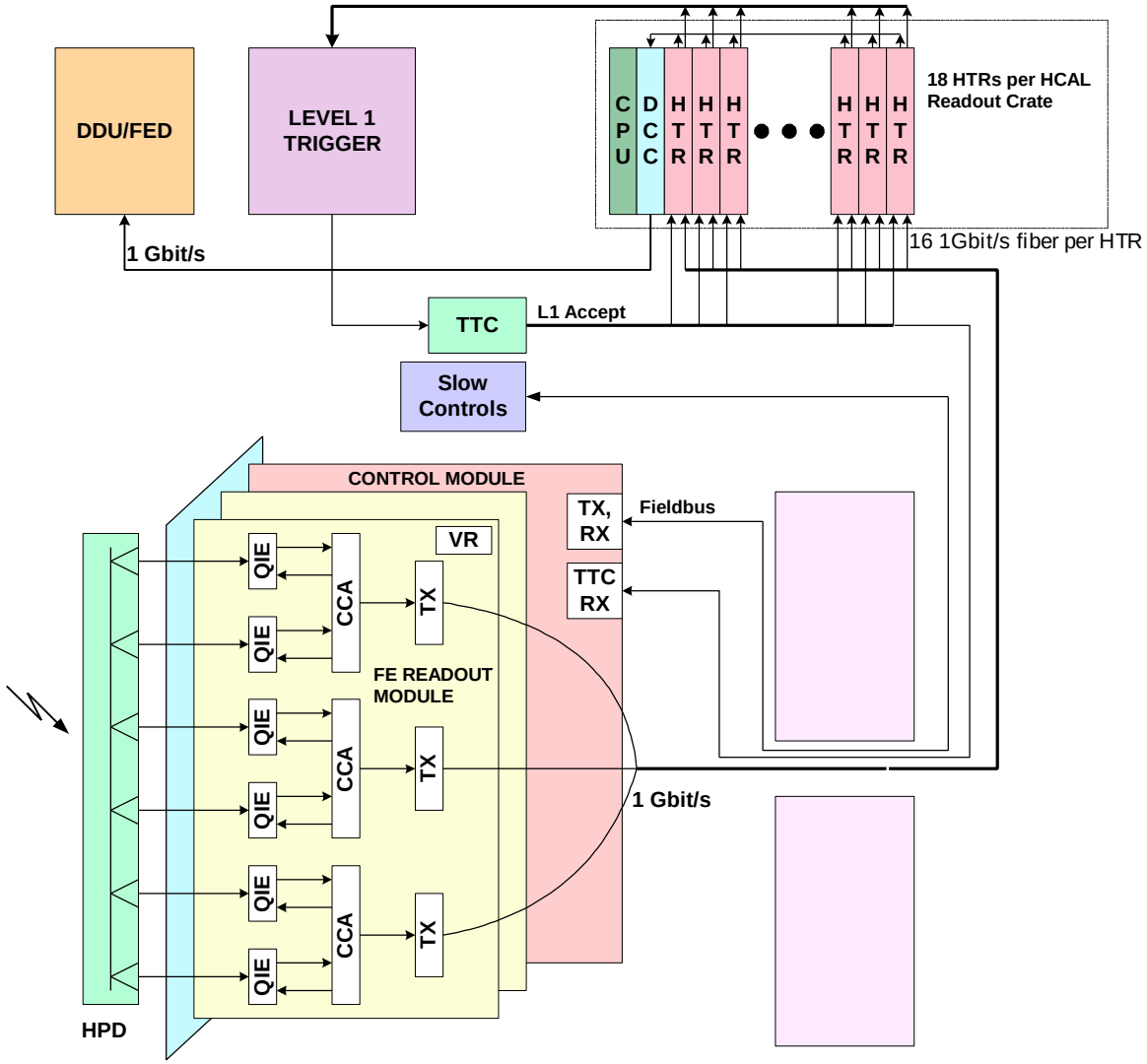
Front End Electronics Organization



Front End System

System	Channel Count	Base Cost
2.1.5 HB	5040	543K
2.2.5 HO	2556	300K
2.3.5 HE	3744	412K
2.5.5 HF	2412	425K
Develop		2172K
Spares		420K
2.x.5	13752	4272K

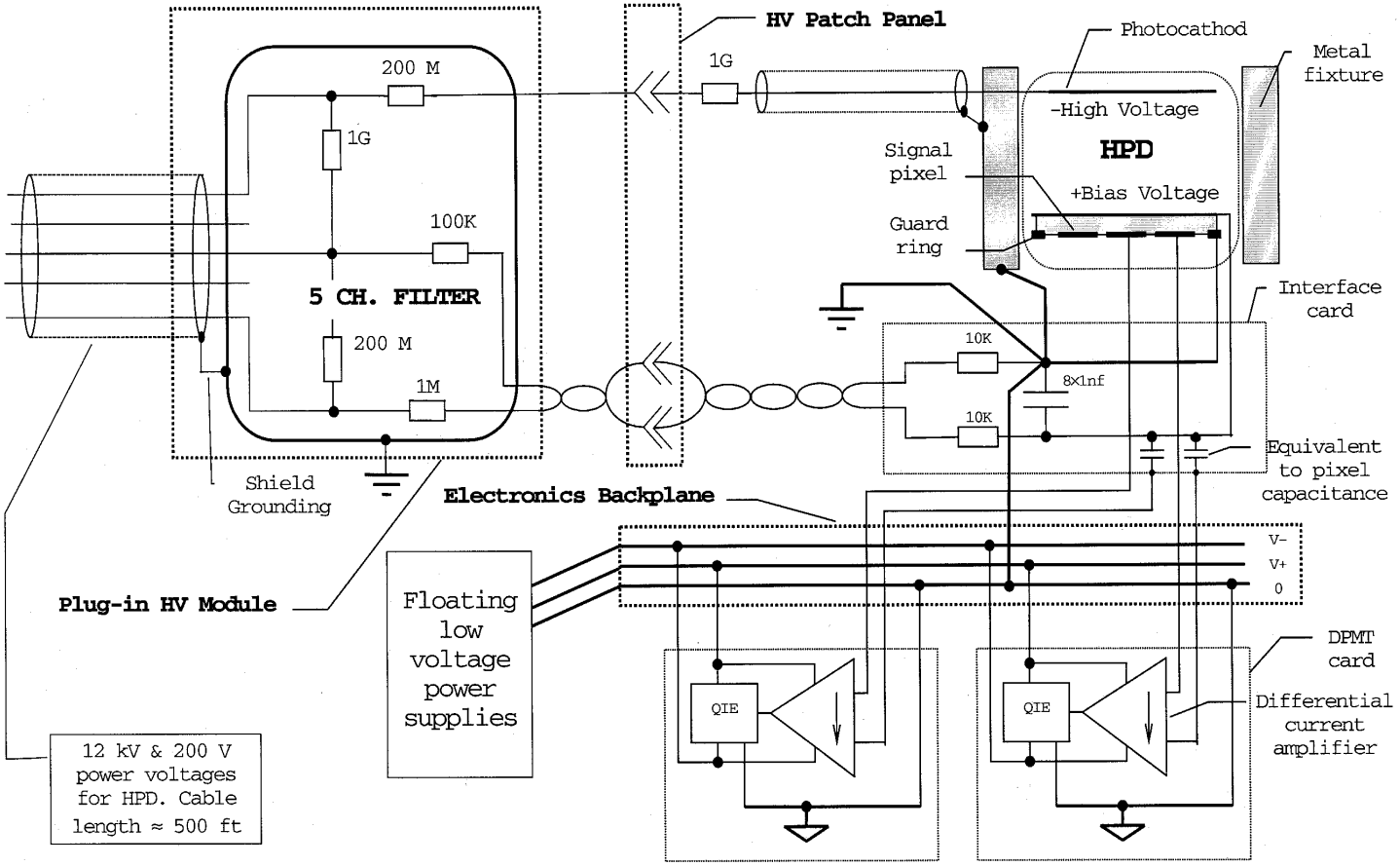
System Overview



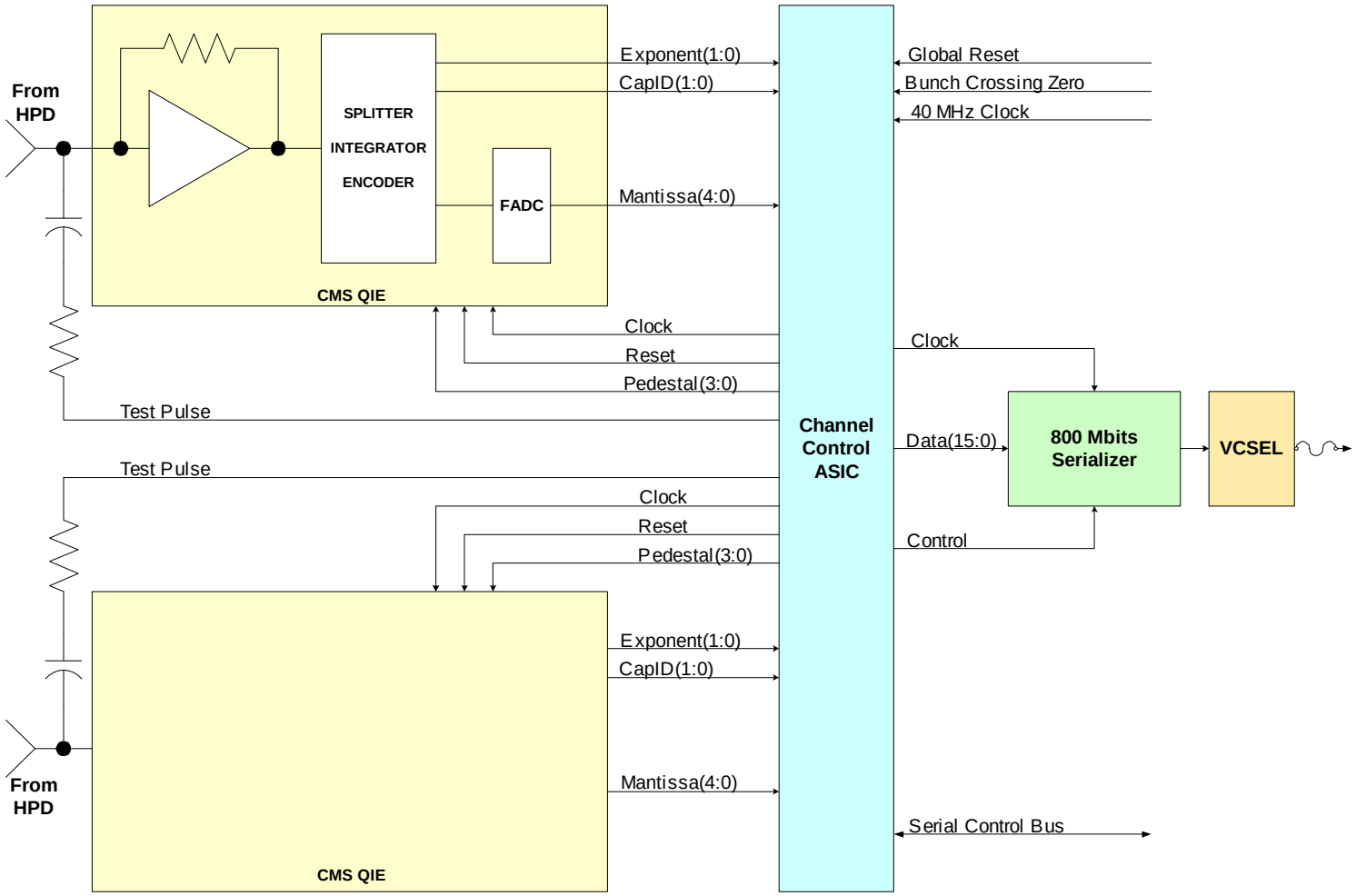
Front End Configuration

3/15/00

HV for HPD and Front End Electronics



Front End Channel Design



Changes since Feb. '99

Front End changes since February 1999

- FADC is now integral part of QIE
- QIE has both non-inverting and inverting input
- Each FE Readout Module will service six channels versus three
- Optical data link uses ECAL's serializer chip and VCSEL

QIE Description

QIE

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

Inverting and Non-inverting Inputs

Internal non-linear Flash ADC

Outputs

- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

QIE Specification

QIE Design Specifications

Clock Speed >40MHz

Must accept both polarity of charge input

Positive Input gain relative to Negative Input = 2.67

Charge sensitivity Lowest Range = 1fC/LSB

In Calibration Mode 1/3 fC/LSB Range 0 only Linear FADC

Maximum Charge = 9670 fC/25ns

Noise 1.5 LSBs in calibration mode, gaussian

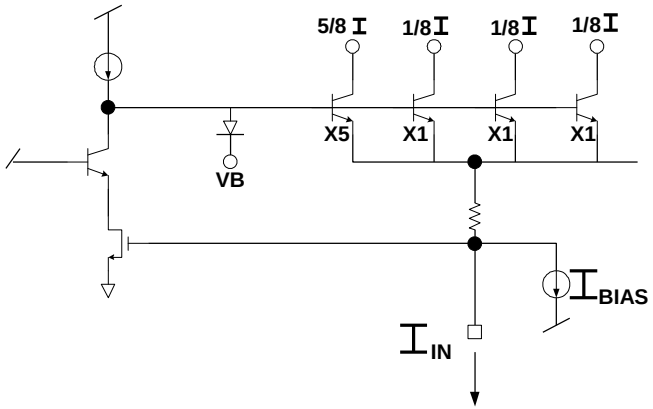
Nominal Pedestal

Calibration Mode nominal Ped = 6.5

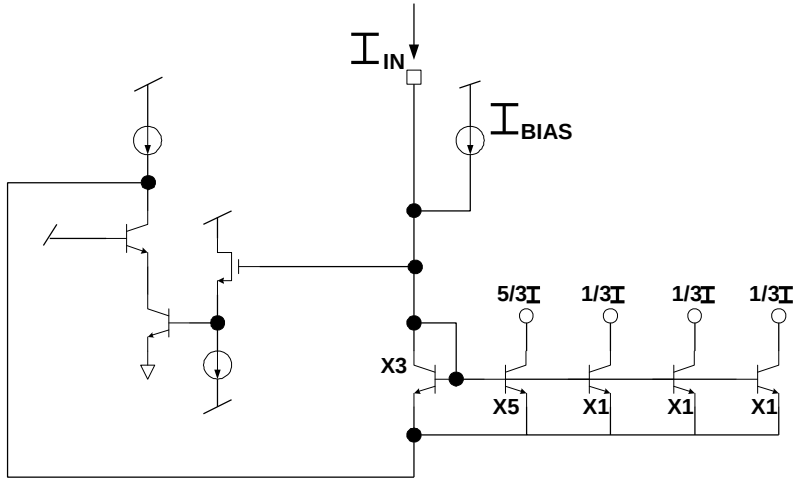
Normal Data Mode Ped = .5

FADC Differential Non-Linearity < .05 LSBs

QIE Input Amplifier and Splitter

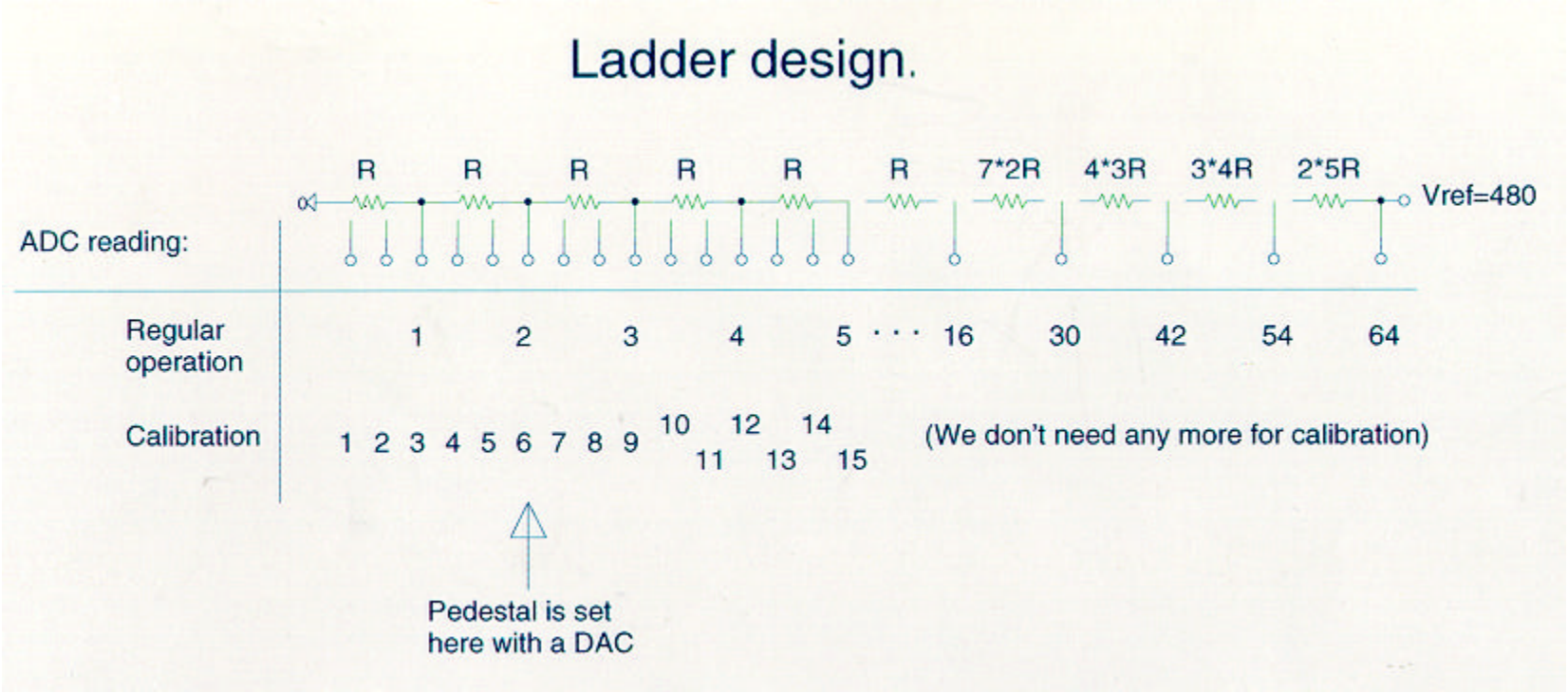


CMS QIE
NON-INVERTING AMPLIFIER/SPLITTER

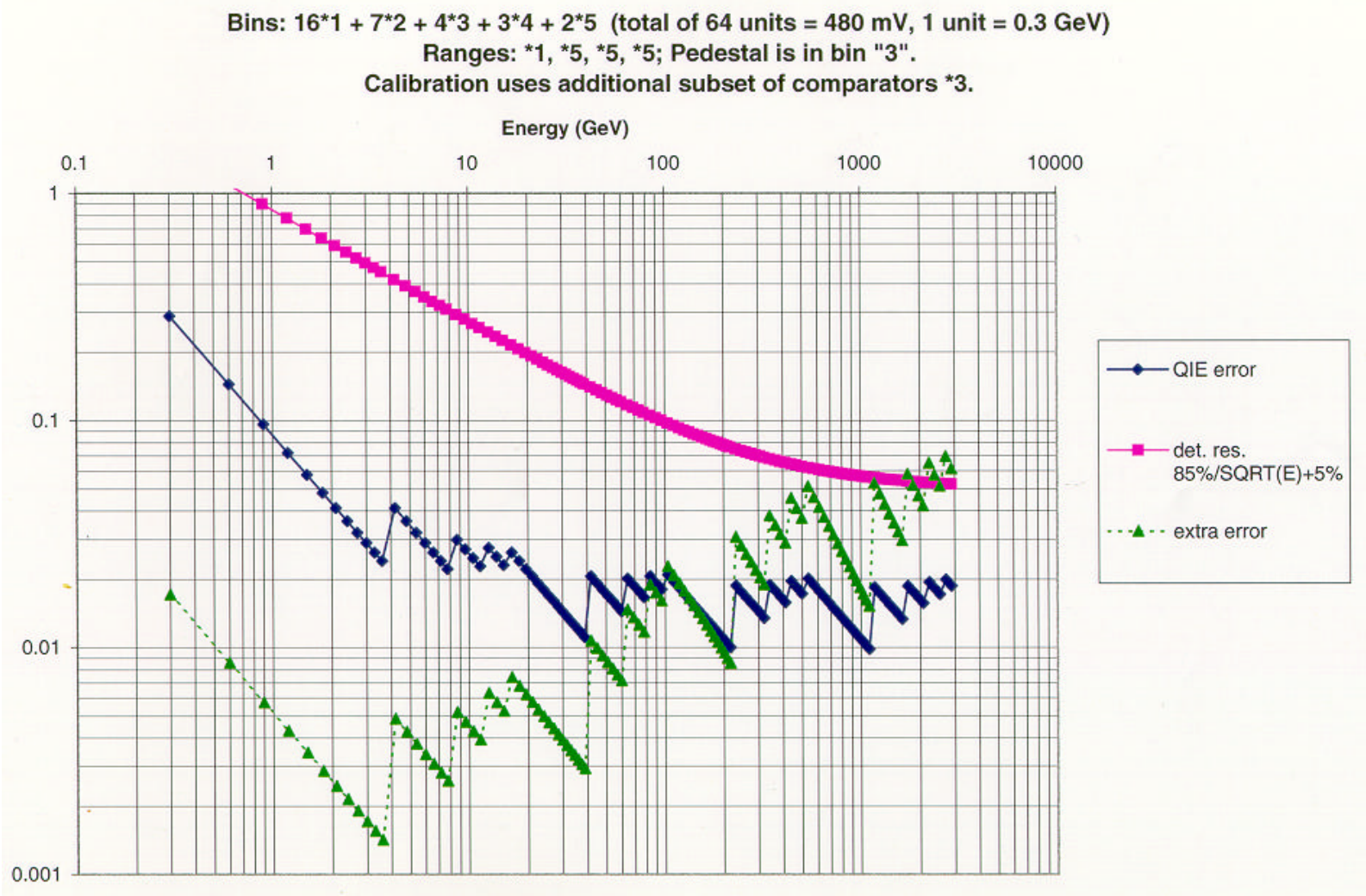


CMS QIE
INVERTING AMPLIFIER/SPLITTER

FLASH ADC Scheme



FLASH ADC Quantization



Channel Control ASIC

The CCA provides the following functions:

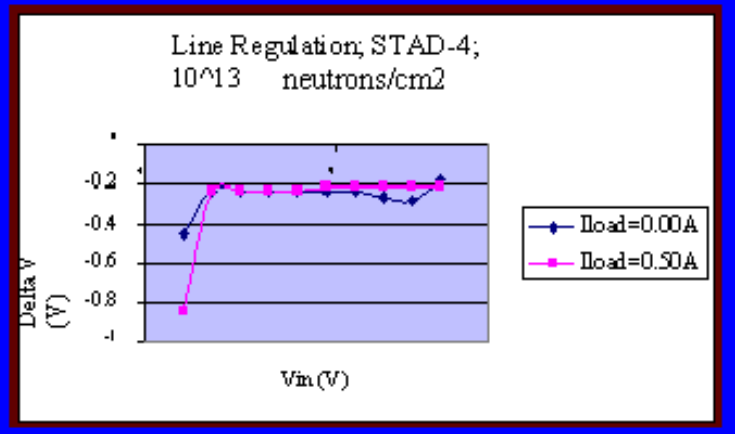
- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to “reset” the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

Rad Tolerant Voltage Regulator

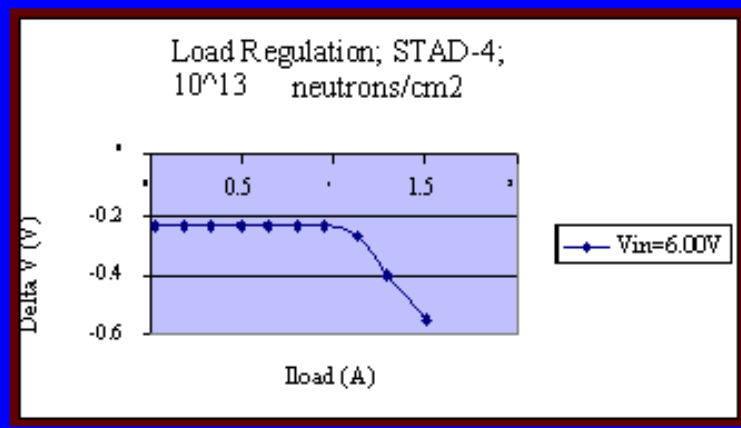
Developed by ST Microelectronics

Specified by CERN RD49

Line regulation ADJ-5V after 10^{13} neutron/cm²



Load regulation ADJ-5V after 10^{13} neutron/cm²



Rad Tolerant Voltage Regulator

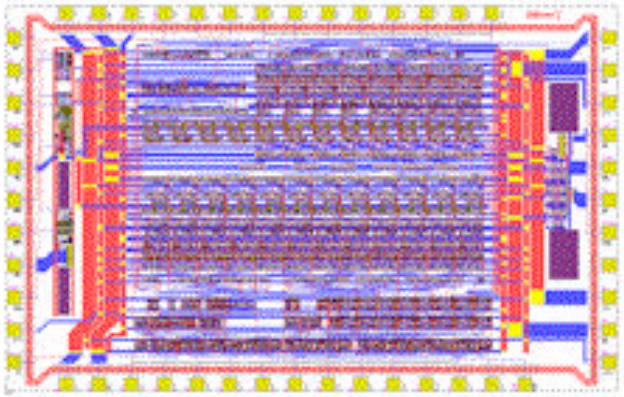
Conclusions

- **Radiation hardness: solved!!**
  - total dose ≥4 Mrad, ≥displacement 5 1013 pr/cm2
  - TBD: extensive statistical measurement
  - How far should we push hardness qualification
- **Performance of the voltage regulator**
  - globally good, revise voltage dropout
  - TBD: output noise
- **Final prototype available in January 2000**
  - **will include positive, 1st silicon for neg**
  - **and overvoltage protection.**

Serializer V2

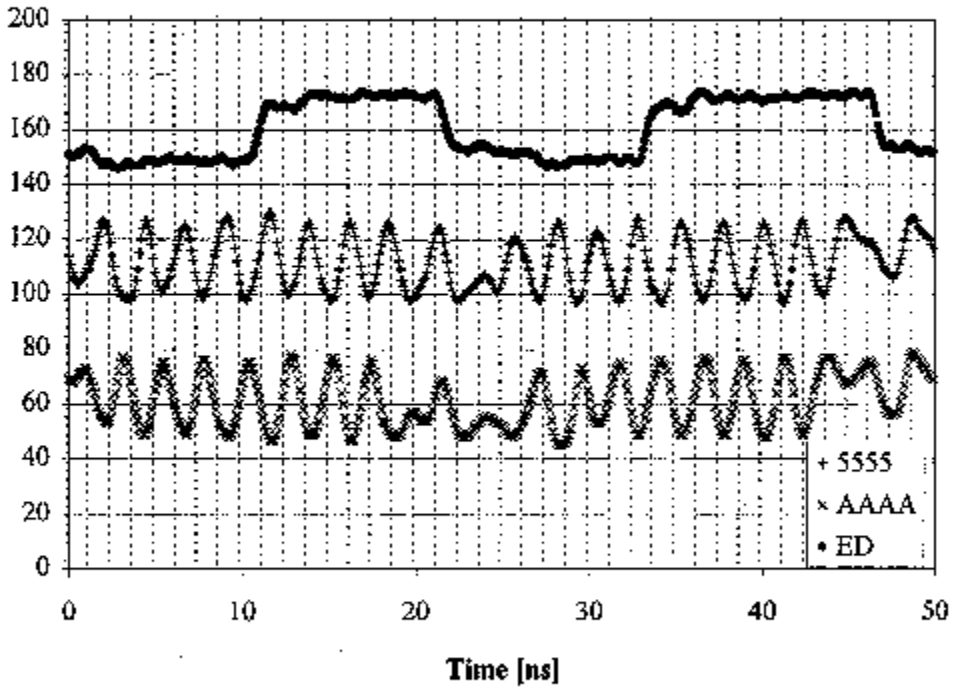
CHFET Fiber Optic Transmitter

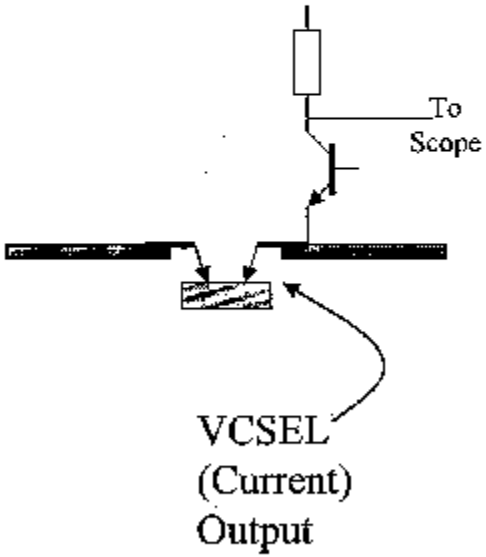
- **Bit serializer with DC line balance protocol and VCSEL driver**
- **Low Power – 120 mW at 800 MB/s including VCSEL**
- **Fabricated in radiation-hard CHFET technology**
- **CIMT protocol – compatible with 16-bit HP G-Link**



Serializer V2

Test at Wafer Probe - Speed Limit





\99cms\ppt\probe at hw P. Denes 11.99

Radiation Testing Plan

Radiation Environment (10yrs)

- neutron fluence: 1.3E11 n/cm^2
- ionizing radiation: 330 rads

Devices to test

- QIE (AMS 0.8 μm Bi-CMOS)
- CCA (HP 0.5 μm bulk-CMOS)
- voltage regulator, fieldbus transceiver, LEDs, PiN-diodes,….

Device Sensitivity

- Bipolars: Displacement Damage, TID, LDR
- CMOS: TID, SEE (SEU + SEL)
  - [SEE immunity -Need LET threshold > 15 MeV-cm^2/mg]

Radiation Test Plans

Previous Testing

- **AMS 0.8 μm Bi-CMOS (VDC&DORIC -Atlas)**
  - Tested to 3E14 n/cm^2 and 10 Mrad
- **HP 0.5 μm bulk-CMOS (Aerospace Corp)**
  - SEL test - LET threshold of 50 MeV-cm^2/mg

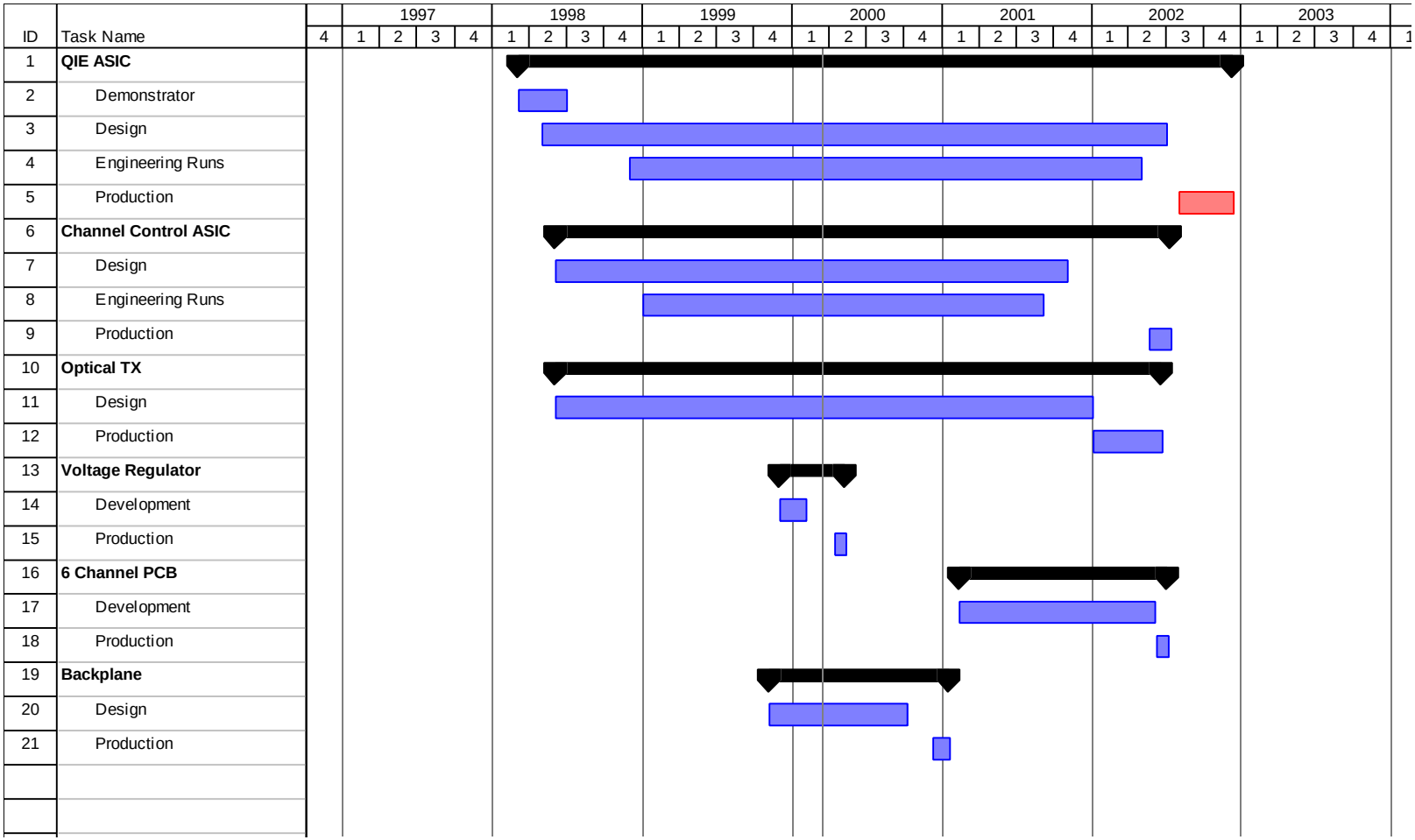
Facility

- **Indiana U. Cyclotron Facility(200MeV protons)**
  - Exposure: 4.3E11 p/cm^2 (2.3 krad TID)

HCAL Elec. Testing (Next 6 months)

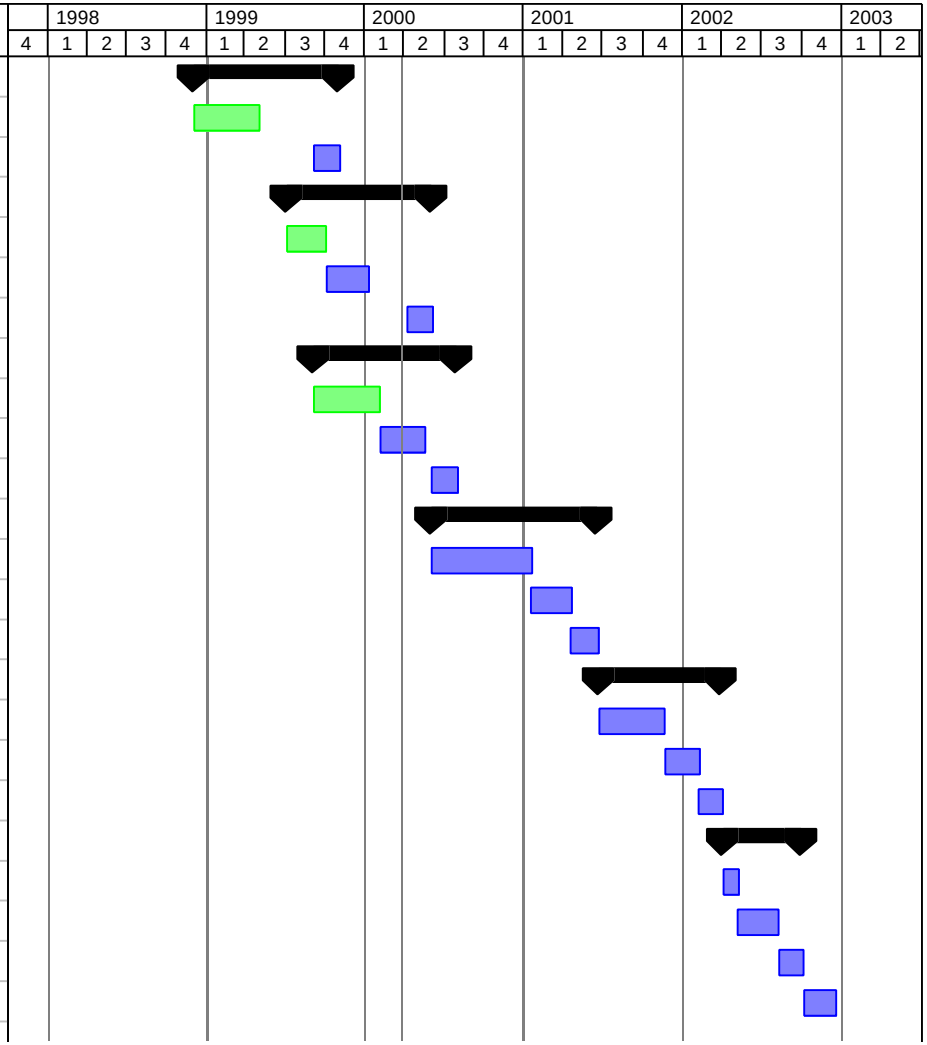
- **Bipolars (Displacement + TID): IU Cyclotron**
  - QIE test device (bipolar splitter)
  - other bipolar devices
- **Bipolars (LDR): Argonne [Co-60 Source]**
  - QIE (bipolar splitter)
- **CMOS (SEE + TID): IU Cyclotron**
  - QIE and CCA test devices (shift registers)
  - voltage regulators, transceivers

FE Production Schedule



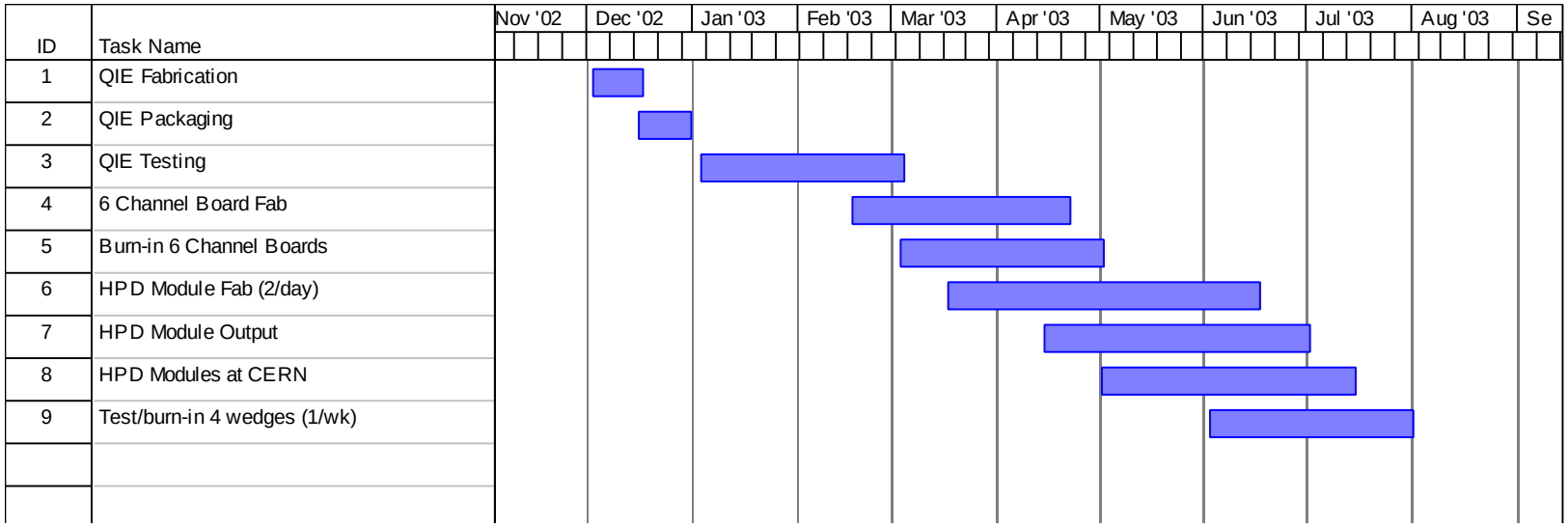
QIE ASIC Schedule

ID	Task Name
1	**Splitter Test Chip**
2	Fab
3	Test
4	**AMP w/ polarity,gain adjust**
5	Design
6	Fab
7	Test
8	**FADC for 4 range splitter**
9	Design
10	Fab
11	Test
12	**Prototype QIE**
13	Design
14	Fab
15	Test
16	**Prototype QIE V2**
17	Design
18	Fab
19	Test
20	**Engineering Run**
21	Design
22	Fab
23	Test
24	Production



Production Electronics Delivery

Schedule which addresses predicted QIE delivery



QIE Alternative

There is concern over the schedule of the CMS QIE Design.

We are looking into using ECAL's EE chip set as a possible back-up.

We do not yet know

- **If this is a viable solution**
- **The cost**
- **The schedule impact**

We hope to understand the details by June/July '00.

FE Electronics - Recent Progress

Past 6 Months

QIE

- Current splitter design submitted and tested
- Input amplifier with polarity and gain adjust has been submitted
- Non-linear Flash ADC design also submitted

Channel Control ASIC

- DLL for timing control submitted and tested
- 1 ns multiplexer design submitted and tested

Serializer

- Decision has been made to use ECAL's Serializer and VCSEL

Backplane

- Prototype being manufactured

FE Electronics – Current Work

Next 6 Months

QIE

- Amplifier with polarity and gain adjust will be evaluated
- FADC design will be tested
- Design work will begin on full version of CMS QIE
- RAD tolerance validation of test structures (AMS process)

Channel Control ASIC

- Serial communication interface will be designed and tested
- RAD tolerance validation of test structures (HP process)
- Additional logic blocks will be designed and tested

FE Electronics – Current Work (Continued)

Next 6 Months

Backplane

- Evaluate clocking distribution
- Evaluate serial communication bus
- Readout box thermal testing

Voltage Regulator

- Test and characterize rad tolerant voltage regulator

Serializer

- Serializer chips are here and under test, only a few minor bugs
- The next batch (~May) will undergo full characterization, bit error rate testing, and integration with final VCSEL packaging

Summary

- **Rebaseline of Front End Electronics is complete**
- **ASIC submissions have begun**
- **Critical path is identified**
- **Everything finishes just in time**